Serial No.: 09/539,206

REMARKS

Claims 1-3 are presently under consideration in the application. Claims 4-8 have been withdrawn from consideration as a result of a previous election. Favorable reconsideration of the application is respectfully requested.

I. REJECTION OF CLAIMS 1-2 UNDER 35 USC §102(b)

Claims 1 and 2 stand rejected under 35 U.S.C. §102(b) based on *Johnson et al.*[1] Applicants respectfully request withdrawal of the rejection for at least the following reasons.

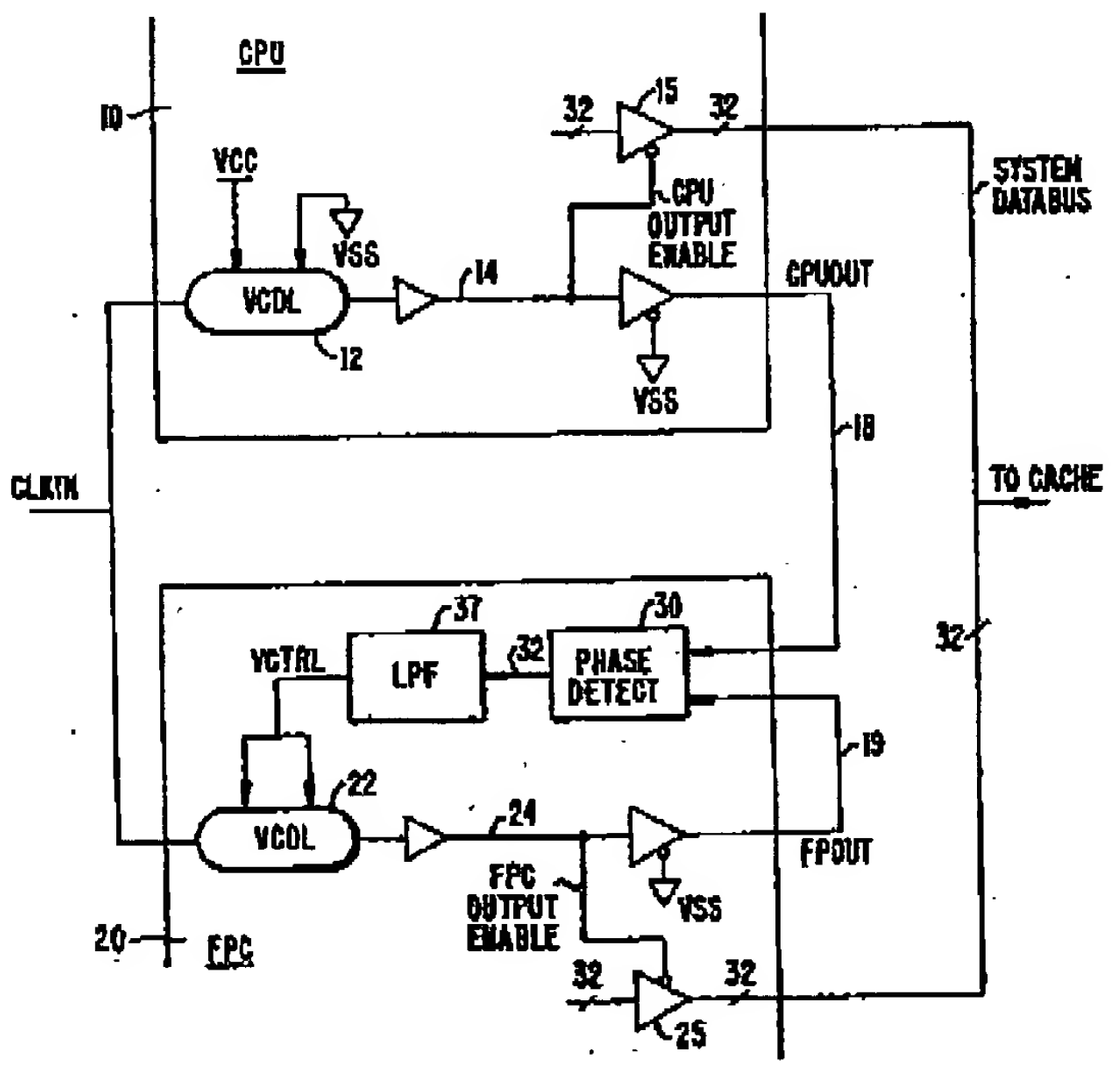

Fig. 1 of Johnson et al.

[1]The Office Action indicates that claims 1-3 are rejected under 35 USC §102(b) based on *Johnson et al.* However, only claims 1 and 2 are addressed in the rejection and claim 3 is addressed separately in the rejection under 35 USC §103(a). Thus, applicants assume the listing of claim 3 as being rejected under 35 USC §102(b) was merely an inadvertent error.

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Regarding Claim 1, the Examiner associates element 12 in *Johnson et al.* (see Fig. 1, reproduced above)as corresponding to the "first delay portion driven by a first driving voltage" as recited in claim 1. Applicants acknowledge that element 12 in *Johnson et al.* is in fact a voltage-controlled delay line. However, the voltage-controlled delay line 12 delays the clock signal supplied thereto by a *fixed* time interval. (See e.g., Col. 2, lns. 32-35). Specifically, *Johnson et al.* teaches that the control voltage inputs for the voltage-controlled delay line 12 are tied to fixed voltages Vcc and Vss. (See, e.g., Fig. 1 and Col. 4, lns. 56-62). Thus, the delay interval will be fixed.

That being said, *Johnson et al.* does not teach or suggest a voltage supplying portion which supplies the first driving voltage to the first delay portion in such a manner that "the first delay time is substantially equal to a clock period of the clock signal" received by the first delay portion, as recited in claim 1. *Johnson et al.* teaches a circuit having a clock signal at 16.7 MHz, thus rendering a clock period of approximately 60 nanoseconds (ns). (Col. 2, lns. 51-55). Fig. 5 of *Johnson et al.* illustrates the operation of the voltage-controlled delay line 12. (Col. 4, ln. 56 - Col. 5, ln. 9). As is shown in Fig. 5, the maximum contemplated delay period for the delay line 12 is approximately 18 ns. This is far short of a clock period (i.e., 60 ns) as required in claim 1 of the present application.

Accordingly, applicants respectfully submit that *Johnson et al.* does not teach or suggest a first delay portion driven in such a manner that the first delay time is substantially equal to a clock period of the clock signal as recited in claim 1. Withdrawal of the rejection of claim 1 is therefore respectfully requested.

Regarding claim 2, the Examiner contends that the "second delay portion" corresponds to the VCDL 22 in *Johnson et al.* However, applicants note that the second delay portion according to claim 2 delays the clock signal by a second delay time and outputs the delayed clock signal. A determining portion determines whether the second delay time is within a predetermined range. A voltage select portion selects, according to the result of the determination of the determining portion, the first driving

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voltage applied to the first delay portion and the second driving voltage applied to the second delay portion.

As noted above, the Examiner considers the VCDL 12 to correspond to the first delay portion. As taught in *Johnson et al.* and discussed above, the voltage VCC provided to the VCDL 12 is *fixed*. Hence, there is *no selection of the first driving voltage supplied to the first delay portion* as recited in claim 2.

Accordingly, *Johnson et al.* also fails to teach or suggest the compensation circuit recited in claim 2. Withdrawal of the rejection is again respectfully requested.

II. REJECTION OF CLAIM 3 UNDER 35 USC §103(a)

Claim 3 stands rejected under 35 USC §103(a) based on *Johnson et al.* in view of *Hase et al.* Applicants respectfully traverse this rejection for at least the following reasons.

Claim 3 depends from claims 1 and 2 and can be distinguished over the teachings of *Johnson et al.* for at least the reasons discussed above. *Hase et al.* does not make up for the above-discussed deficiencies in *Johnson et al.* Applicants respectfully request withdrawal of the rejection.

III. CONCLUSION

Accordingly, all claims 1-3 are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

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Should a petition for an extension of time be necessary for the timely reply to the outstanding Office Action (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

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DATE: September 17, 2004

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